

Designing with the Spartan 6 Family

Ref : 004851A

Duration : 2 days

OBJECTIVES

- Learn how to effectively utilize Xilinx Spartan®-6 architectural resources.
- Master the CLBs and different type of slices structure.
- Master clocks resources (DCM, PLL and also global , horizontal, area and IO clocks).
- Design effectively with block RAM and block DSP.
- Effectively use I/O blocks especially with SERDES blocks.
- Know the memory controllers.
- Proper VHDL coding techniques.
- Introduction to the integrated hardware resources (Multi-Gigabit Transceivers and PCI-e)

RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGAs design (002572A)
- Designing for performance, ISE (002833A)
- Designing a LogiCore PCI-Express system (004552A)
- Designing with Multi-Gigabit Rocket-IO transceivers (002843A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Basic knowledge FPGAs architectures.
- A successful first experience of designing an VHDL or Verilog based FPGA.

PRACTICAL LABS

Software configuration:

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration:

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Spartan-6 family overview
- CLB and Slices architecture
- HDL Coding techniques
 - Exercise
- Memory Resources
- DSP Blocks

- Exercise
- I/O Blocks

2nd day

- Exercise
- Clocking Resources and management
- Exercise
- Memory Controller
- Introduction to dedicated resources (MGT et PCI-e)

DOCUMENTATION

Training manuals in print will be given to attendees during training.