

## Spartan-6, ISE 11

Ref : 004851A

Duration : 2 days

### OBJECTIVES

- Learn how to effectively utilize Xilinx Spartan®-6 architectural resources.
- Master the CLBs and different type of slices structure.
- Master clocks resources (DCM, PLL and also global , area and IO clocks).
- Design effectively with block RAM and block DSP.
- Effectively use I/O blocks especially with SERDES blocks.
- Know the memory controllers.
- Proper VHDL coding techniques.
- Introduction to the integrated hardware resources (Multi-Gigabit Transceivers and PCI-e)

### RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGAs design (002572A)
- Designing for performance, ISE (002833A)
- Designing a LogiCore PCI-Express system (004552A)
- Designing with Multi-Gigabit Rocket-IO transceivers (002843A)

### PARTNERS

- This training course is approved by XILINX

### PREREQUISITES

- Basic knowledge FPGAs architectures.
- A successful first experience of designing an VHDL-based FPGA.

### PRACTICAL LABS

#### Software configuration:

- Xilinx ISE Design Suite 11.1 Logic Edition

#### Recommended Hardware Configuration:

- Intel Core 2 or equivalent
- Windows XP
- 1 GB available on hard drive after softwares install
- At least 1GB of RAM
- Display Resolution : at least 1024 x 768
- For on site training, we need a video projector

Authorized  
Training Provider

### Contact

Tel : 05 62 13 52 32  
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training@mvd-fpga.com

Course also available  
customized

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

### TOPICS

#### 1<sup>st</sup> day

- Spartan-6 family overview
- CLB and Slices architecture
  - Exercise
- Memory Resources
- DSP Blocks
  - Exercise
- I/O Blocks

#### 2<sup>nd</sup> day

- I/O Blocks (continuation)
- Clocking Resources and management
  - Exercise
  - Memory Controller
- VHDL Coding techniques
  - Exercise
- Introduction to dedicated resources (MGT et PCI-e)

### DOCUMENTATION

Training manuals in print will be given to attendees during training.