

Designing with the Virtex 6 Family

Ref : 004852A

Duration : 2 days

OBJECTIVES

- Learn how to effectively use Xilinx Virtex™-6 architectural resources.
- Understand the CLBs and different type of slices structure.
- Understand clocks resources (MMCM and also global, horizontal, regional and IO clocks).
- Design effectively with block RAM and block DSP.
- Effectively use I/O blocks especially with SERDES blocks.
- Know the memory controllers
- Proper VHDL coding techniques.
- Introduction to the integrated hardware resources (Multi-Gigabit Transceivers, PCI-e, MAC Ethernet and System Monitor)

RELATED COURSES

- VHDL logical synthesis and simulation for Xilinx FPGAs Design (002572A)
- Designing for performance, ISE (002833A)
- Designing a LogiCore PCI-Express system (004552A)
- Designing with Multi-Gigabit Rocket-IO transceivers (002843A)

PARTNERS

- This training course is approved by XILINX

PREREQUISITES

- Basic knowledge FPGAs architectures.
- A successful first experience of designing an VHDL or Verilog based FPGA.

PRACTICAL LABS

Software configuration:

- Xilinx ISE Design Suite 13.1 Logic Edition

Recommended Hardware Configuration:

- Intel Core 2 or more recent
- Windows XP or 7
- 1 GB Free disk after software installation
- At least 2Go RAM
- Minimum Display resolution : 1024 x 768
- On Site training : video projector



Contact

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Course also available
customized on site

Next sessions, see : <http://www.mvd-training.com/en/schedule.html>

TOPICS

1st day

- Virtex-6 family overview
- CLB and Slices architecture
- VHDL Coding techniques
 - Lab : CLB resources
- Memory Resources
- DSP Blocks
 - Lab : DSP resources

- I/O Blocks

2nd day

- I/O Blocks (continuation)
- Lab : I/O Resources
- Clocking Resources and management
 - Lab : Clocking Resources
- Memory controller
- Introduction to dedicated resources (MGT, PCI-e and EMAC)

DOCUMENTATION

Training manuals in print will be given to attendees during training.