
USB 3.0

Ref : 004853A

Duration : 1 day

OBJECTIVES

- The course details the new dual architecture of USB 3.0 implementation
- An architectural view of an USB 3.0 is analysed
- All packets and transfer are studied layer by layer
- The course focuses on the bus enumeration sequence

RELATED COURSES

- USB 2.0 bus (002606A)

PREREQUISITES

- Knowledge of USB 2.0 is mandatory

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Course also available
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

TOPICS

SYSTEM ARCHITECTURE

- objectives of USB 3.0
- topology with a dual architecture
- differences between USB 2.0 and USB 3.0
- the new mechanical
- the USB 3.0 architecture

DATA FLOW MODEL

- Transaction Packet (TP)
- Data Packet (DP)
- Link Management Packet (LMP)
- ITP (Isochronous Timestamp Packet)
- Transfer model

PHYSICAL LAYER

- scrambling
- 8b/10b coding scheme
- elastic buffer
- receiver detection
- Low Frequency Periodic Signaling (LFPS)
- link initialization and training
- eyes diagrams
- loopback BERT

LINK LAYER

- Link packet format
- Link flow control
- Header Sequence Number Advertisement
- Rx Header Sequence Credit Advertisement

- Transfert packet
- link timers
- example of a sequence with a CRC16 error
- Link Training and Status State Machine (LTSSM)

PROTOCOL LAYER

- End-to-end communication
 - Rules
 - Flow control
- Device notification
- Isochronous transfer
- Bulk transfer with stream
- Control transfer
- Interrupt transfer

DEVICE

- New descriptors
 - BOS
 - USB 2.0 Extension
 - SuperSpeed USB Device
 - Container ID
 - Interface Association
 - SuperSpeed Endpoint Companion
- New commands
 - SET_ISOCH_DELAY
 - SET_SEL

HUB

- Routing mechanism
- Hub Architecture
- The new descriptors of USB 3.0 hub

DOCUMENTATION

- Training manuals will be given to attendees during training in print.