

## QorIQ P20x0

Ref : 004855A

Duration : 4 days

### OBJECTIVES

- The course focuses on the Ocean crossbar that interconnects e500, RapidIO, DDR SDRAM, PCI and external bus
- Cache coherency protocol is introduced in increasing depth
- The 64-bit e500 core is viewed in detail, especially the SPE that enables Floating point and vector processing
- The boot sequence and the clocking are explained
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers

### RELATED COURSES

MVD Training offers additional trainings

- PCI express (ref 003279A)
- USB2.0 (002606A) and USB3.0 (ref 004853A)
- Ethernet (003367A)

How to use LTIB for Linux application

### PREREQUISITES

- Basic knowledge about processors

### PARTNERS

- This training course is approved by FREESCALE

**WIND RIVER****NeoMore**

### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### INTRODUCTION TO THE QorIQ20x0 [2-hours]

- Implementation examples
- Internal data flows, OCEAN switch fabric, packet reordering
- Address map, ATMU
- Local vs external address spaces, inbound and outbound address decoding
- Accessing CCSR memory from external master
- System performance monitor

#### THE e500 CORE [10-hours]

- Differences between the new Book E architecture and the classic PowerPC architecture
- The instruction pipeline : dual-issue superscalar control, out-of-order execution, 12-entry instruction queue, 14-entry completion queue
- Execution units : 2 Simple Integer Units and 1 Complex Integer Unit
- Dynamic branch prediction using a 128-set 4-way set associative Branch Target Buffer
- Execution timing, rename register operation, instruction serialization, instruction scheduling guidelines
- The first level MMU and the second level MMU, consistency between L1 and L2 TLBs, snooping of TLBs, TLB software reload, page attributes WIMGE
- Process protection, PID registers and sharing
- The L1 caches, PLRU replacement algorithm, 8-way set associativity, cache block and unlock APU
- Cache coherency : MEI vs MESI state machine
- Allocation of data transferred by external masters into the cache
- ECM: e500 coherency module
- The Core Complex Bus : high speed on-chip local bus with data tagging
- Load store unit, data buffering between LSU and CCB : the LMQ, the store queue, the castout queue, store miss merging and store gathering, memory access ordering, lock acquisition and import barriers
- Signal Processing APU (SPU) : implementation of the SIMD capability without using a separate unit
- PowerPC EABI : sections, C-to-assembly interface
- Book E exception handling, critical versus non critical,
- Core timers : Dec, TB, FIT and Software Watchdog
- Configurable context switching for GPRs, SPRs and some additional registers
- Power management, disabling the timer, interrupts and power management, snooping in the power-down state
- Performance monitoring, counting of events

- JTAG emulation, real time trace when the e500 core executes cached instructions
- Watchpoint logic, triggering capabilities based on user programmable events

#### RESET, CLOCKING AND INITIALIZATION [3-hours]

- Platform clock
- Power-on reset sequence, use of the I2C interface to access serial ROM
- Power-on reset configuration
- Boot page translation
- Power management

#### Open PIC [2-hours]

- PIC architecture
- Interrupt Sources
- Programming model
- Software implementation

#### BASICS OF HARDWARE IMPLEMENTATION [4-hours]

- DDR-SDRAM controller
- Local bus controller
- PCI express
- Software implementation of these units

#### ENHANCED- TSECs [6-hours]

- 802.3 specification fundamentals: the 3 layers PHY, MAC and control
- Frame format with and without VLAN option
- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast
- Direct queuing of four flows

#### INTEGRATED DMA CONTROLLER [2-hours]

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency
- Ability to start DMA from external 3-pin interface

### DOCUMENTATION

Training manuals will be given to attendees during training in print.