

PCI BUS 3.0

Ref : 002596A

Duration : 3 days

OBJECTIVES

- The training has been designed from the PCI3.0 specification
- Transfer protocol understanding with a lot of labs with the assistance of a Lecroy analyser
- A software routine has been developed to show how to access the configuration space
- PCI initialization program description : interrupt requests allocation, memory regions allocation
- PCI performance tuning : selecting optimized LT value, appropriate master priority, enabling fast-back-to-back
- The course emphasizes the host bridge operation especially the management of PCI accesses targeting cache enabled regions



PREREQUISITES

- Experience of a digital bus is recommended
- Experience of a 32-bit processor is recommended

RELATED COURSES

- MVD also offers a PCI Express training, reference 003279A
- A specific course details the implementation of the Xilinx PCI logicore (reference 002841A)



Contact

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Course also available
customized

TOPICS

OVERVIEW

- PCI specifications history
- PCI bus features
- PCI device types
- Technological introduction
- Architecture of recent PCs

PCI DEVICE ARCHITECTURE

- Information buffering
- Buffer management
- Prefetchable vs non-prefetchable memory ranges
- Synchronization rules : Producer / consumer model
- PCI bus limitations

TRANSFER PROTOCOL

- Transfer basics
- Pinout, signal classes
- Arbitration
- Data transfer protocol
- Address decoding in IO, MEM and CFG spaces
- Master and Target initiated terminations
- Parity control
- Shared resource management
- Bus analyse, benefit of a bus analyser / exerciser

INTERRUPTS AND RESET

- PCI interrupts
- Interrupt acknowledge transaction
- Interrupt sharing
- Message Signaled Interrupts
- Reset, operating states :

ELECTRICAL SPECIFICATION

- Switched wave switching vs Incident wave switching
- Static specification
- Dynamic specification : 33 MHz and 66 MHz
- Clocking, Decoupling
- Compliance checklists

CONFIGURATION SPACE

- Configuration space mappings and register description
- PCI MEM and PCI IO mappings building
- Capability list
- Configuration transactions, IDSEL routing
- Local vs distant CFG transaction
- Generation of config transactions

PCI-TO-PCI TRANSPARENT BRIDGES

- Bus numbering
- Address decode, transaction forwarding rules
- Distant configuration cycles
- Error management

CACHE COHERENCY

- Cache and snooping basics
- Cacheability of RAM accessed by the host CPU through PCI
- PCI masters accessing the host memory
- PCI agent processor accessing the host memory

PCI BASED INDUSTRIAL SPECIFICATIONS

- Passive bus PICMG PC
- CMC/PMC mezzanine boards, BUSMODE pins management
- CompactPCI introduction
- PC104+, PC.MIP introduction

DOCUMENTATION

Training manuals will be given to attendees during training in print.

COMPLEMENTARY INFORMATIONS

Web Site : <http://www.mvd-fpga.com>
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