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## VME64 BUS

Ref : 002599A

Duration : 4 days

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### OBJECTIVES

- This course is based on the ANSI-VITA 1 1994 specification and ANSI-VITA 1.1 extensions
- The new 2eSST protocol is also described
- The training highlights synchronization methods like mailbox generally used in VME based calculators
- The daisy-chain acknowledge mechanism is viewed in detail
- Shared resource management is also emphasized
- The training shows how to configure a VME backplane
- After having reminded the 68K interrupt management, the VME priority interrupt bus is described
- VME timing diagrams are studied with the assistance of the VSYSTEMS analyser board
- The course focuses on the configuration space specified in the VME64 and VME64x standards

### PREREQUISITES

- Experience of a parallel digital bus is recommended

### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

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### TOPICS

#### INTRODUCTION TO THE VME BUS

- VME based calculator architecture
- Connectors pinout
- The four bus parts

#### THE ARBITRATION BUS

- Explanation of the daisy-chain acknowledge mechanism
- RRS, PRI and ONE Arbiter options
- RWD, ROR, FAIR requester options
- Arbitration sequence analysis

#### THE DATA TRANSFER BUS

- Byte locations accessed during a data transfer
- Address pipelining
- Burst transfers
- Address Only transactions
- BTO timer utility
- Shared resource management

#### THE INTERRUPT BUS

- Interrupt generator structure
- Interrupt handler structure
- Status/ID read cycle
- ROAK and RORA interrupt generator options

#### THE UTILITY BUS

- SYSFAIL management
- Reset timing diagram
- Power control

- Auto system controller

#### ELECTRICAL SPECIFICATION

- The 5 signal types
- Bus driving and receiving requirements
- Noise margins
- Board powering, current ratings for power pins
- Line terminations
- The ETL transceiver logic required for 2eSST

#### THE CONFIGURATION SPACE

- Determination of the mapping of the A24 config space
- Detail of the CR and CSRs
- Auto slot ID mechanism

#### VME64x EXTENSIONS

- New P0/J0 connector
- P1/J1, P2/J2 connectors pinouts, rows z and d pin assignments
- Live insertion support
- EMC front panel and subbracks
- ESD protection
- ETL technology
- 2eVME protocol

#### 2eSST PROTOCOL

- 3U and 6U implementations
- Broadcast transfers
- Source synchronous transfers, data centered strobes
- Skew calculation

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.