RapidIO

Ref : 002602A **Duration : 3 days**

OBJECTIVES

- The course covers features up to the RapidIO 2.1 specification, like end-to-end flow control, multicast programming and data streaming Packet switching benefits compared to shared busses are highlighted
- The course explains the various traffic types that RapidIO supports : Input / output, Message and GSM
- Mechanisms like error recovery and flow control are explained through various sequences
- CC-NUMA cache coherency mechanism is studied
- The course describes the discovery sequence required to initialize the switches
- Details of RapidIO interfaces present in Freescale and Tundra devices are provided to explain how theoretical statements are actually implemented

PREREQUISITES

- Experience of a bus

RELATED COURSES

- The MPC8548 has a RapidIO port (course 002881A)
- The MPC8641D has a RapidIO port (course 003771A)

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Course also available customized

Next sessions, see : *http://www.mvd-fpga.com/en/formationsCalend.html*

TOPICS

THE TRANSITION TO PACKET SWITCHING

- PCI, PCI-X bus limitations
- Solutions to increase the performance : differential transmission, packet switching, gigabit serdes

INTRODUCTION TO RapidIO

- System view
- Layer model, features of logical, transport and physical layers
- Purpose of control symbols
- Request / response sequence

THE INPUT / OUTPUT LOGICAL TRAFFIC

- Accessing memory mapped address ranges
- Accessing the configuration space
- Atomic and maintenance transactions
- Transaction ordering, Transfer efficiency calculation

THE MESSAGE PASSING LOGICAL TRAFFIC

- Interconnection of host domains
- Message vs doorbell, Transfer efficiency calculation
- Detail of message passing implementation in Freescale netcomm devices

CACHE COHERENCE

- Cache basics and coherency
- Data shared by DMA and CPU through a RapidIO fabric
- Data shared by CPUs connected to a RapidIO fabric
- GSM transactions, coherence domains
- The CC-NUMA approach
- Analysis of various cache coherency sequences

LOGICAL LAYER FLOW CONTROL

- Types of congestion
- Controlled flow list
- XON-XOFF controls on transaction request flows
- XON-XOFF counters
- Ordering rules

PACKET PRIORITY AND FLOW CONTROL

- Transaction ordering rules
- Mapping flowID into 2-bit priority
- Receiver based flow control, retry mechanism
- Transmitter based flow control, management of transmit credits
- Deadlock prevention

THE TRANSPORT LAYER

- Common transport layer
- Packet routing through the network based on destination ID
- Programming interface to read / write the routing tables
- Multicast extensions (RapidIO 1.3)
- Hardware support for the duplication of posted write packets
- Setting a list of egress ports in a multicast mask list
- Associating a destination ID with the multicast mask

SYSTEM BRINGUP

- System exploration and initialization
- Winning host
- System enumeration API
- Enumeration time-out
- Hardware abstraction layer

OVERVIEW OF THE PHYSICAL LAYER

- Alignement rules
- Packet acknowledgement
- Control symbols vs packet
- Multicast event

ERROR MANAGEMENT

- Packet protection through CRC
- Early processing of packets
- Study of various sequences explaining the ability of RapidIO to recover from errors automatically by hardware
- Software aspects, link maintenance request and response
- RapidIO 1.3 added requirements in physical and logical layers
- Error reporting thresholds
- Port behaviour when error rate failed threshold is reached
- Drop packet enable
- System software notification of errors

DATA STREAMING LOGICAL SPECIFICATION

- Data path vs control path requirements
- Mechanism of transporting an arbitrary protocol over a standard RapidIO interface
- Traffic streams
- Support for PDU of 64 kB through segmentation and reassembly
- Class of services and virtual queues
- IP over RapidIO

THE LP-LVDS 8/16 INTERFACE OVERVIEW

- Transfer protocol, packet and control symbol delineation
- Insertion of symbols within packets
- Use of eye diagram to specify the electrical interface
- Training pattern

THE LP-S INTERFACE OVERVIEW

- Features or sublayers PCS and PMA
- The 8b/10b encoder / decoder
- Symbol and packet delimitation
- Idle sequence, Lane synchronization
- Retimers and repeaters
- Use of eye diagram to specify the electrical interface