

OBJECTIVES

- Give to the project manager an in depth presentation to be able to use efficiency all the resources of the component
- Give to the developer a good understanding to set up easily all the internal functions
- Study the global architecture in details : (everything concerning the user is covered)
 - ✓ To obtain the best performance based on the different flows of data crossing the XBAR, the help of numerous DMA channels and a powerful interrupt controller
 - ✓ To manage power
 - ✓ To use efficiently all the protection mechanisms and secure resources for your algorithms

RELATED COURSES

- CAN bus training (ref. 002601A)
- C language for real-time and embedded applications (ref 002603A)
- eTPU programming (ref. 003199A)

PREREQUISITES

- Experience of a microcontroller is recommended
- This training is adapted to the electronics and programmers engineers confronted with the problems of the implementation of this processor

PARTNERS

- This training course is approved by Freescale


WIND RIVER

Contact

Tel : 05 62 13 52 32
 Fax : 05 61 06 72 60
 training@mvd-fpga.com

Course also available
 customized

Next sessions, see: <http://www.mvd-training.com/en/schedule.html>

TOPICS
MPC555X OVERVIEW

- Automotive MPC55XX roadmap
- Internal architecture of the Copperhead (MPC5554)
- Functional pin multiplexing
- Memory map, internal register space

e200 CORE

- Differences between the new Book E architecture and the classic PowerPC architecture
- The instruction pipeline
- Integer and floating point execution units
- SPE instruction set, signal processing capability, new data types
- Vector and scalar floating point
- The MMU, 32-entry fully associative TLB, page size selection
- Hardware assist for TLB miss exception
- Page attributes WIMGE
- Process protection, variable number of PID registers and sharing
- TLB initialization
- The 32-kB unified L1 cache, pseudo round-robin replacement algorithm, 8-way set associativity
- 8-entry store buffer
- Cache-related instructions
- ABI : sections
- Book E exception handling
- Core timers
- Nexus emulation
- Watchpoint logic

THE INTERRUPT CONTROLLER

- Up to 504 on-chip module interrupt sources
- Software vs hardware vector mode
- Hardware acceleration for ISRs : use of 9-bit vectors
- Preemption, priority management
- External IRQs

HARDWARE IMPLEMENTATION

- FMPLL
- Configuration pins
- Reset configuration half word
- Boot assist module, 4 different boot modes
- MMU configuration after BAM executes
- Initialization sequence
- External bus interface, pinout

- Memory controller with support for SDR flash and SRAM
- Compatibility with the external bus of the MPC5XX
- Support for external master accesses to internal addresses
- Burst support
- Chip-select programming

ON-CHIP MEMORIES

- 2 MB on-chip flash
- Integrated ECC
- Censorship protection
- Read while write operation
- Erase and program sequences
- 111 kB on-chip SRAM : general purpose SRAM, cache and eTPU RAMs

eDMA AND CROSSBAR

- Autonomous IO control
- Parallel memory bus architecture, concurrent accesses
- Programmable master priorities on a per-slave basis
- 64 independent channels with link capability
- Parking on slave ports
- Transfer control descriptors, inner and outer loops, modulo feature
- Scatter / gather feature
- DMA channel arbitration
- DMA error reporting

THE eTPUs

- Real time hardware events processing, scheduling, priority scheme
- Microengine operation
- New arithmetic, logical and control instructions
- Angle clock hardware
- DMA support
- Dual eTPU shared resources
- Introduction to the eTPU functions QOM, NITC, PWM, SIOP, UART
- Channel service max latency time calculation
- eTPU development tools, Ashware debugger

eMIOS

- Introduction to time functions supported by the 24 unified channels
- DMA request per channel
- Pin serialization / deserialization
- eMIOS interrupt requests

Course description (ref. 003151A)**Duration: 4 days**

- Double action submodules
- PWM submodules, center aligned PWM
- Windowed programmable time accumulation
- Quadrature decode

eQADC

- Analog inputs multiplexing
- 12-bit AD resolution
- Queue management, trigger sources
- Conversion queue priority scheme
- Conversion cycle times
- eQADC command / data flow
- Hardware interface
- ADC error correction

DSPI

- SPI protocol explanation, master / slave operation
- Command queue

DOCUMENTATION

Training manuals will be given to attendees during training in print.

- Flexible programming transfer attributes on a per-frame basis
- Transmit and receive sequences

eSCI

- UART basics
- Double buffering
- Wake up mode
- Transmit and receive sequences
- Support for LIN master operation

The FlexCAN controllers

- CAN protocol basics
- Message buffer structure
- Mask registers
- Listen-only mode capability
- Receive and Transmit processes
- Error counters