

## Mobile GT MPC52xx IMPLEMENTATION

Ref : 003152A

Duration : 5 days

### OBJECTIVES

- The course explains how to design a MPC52xx board
- DDR SDRAM operation is described in order to understand the memory controller programming
- The 603e core is studied in detail, especially the MMU
- The course provides examples of internal peripherals software drivers
- Fast Ethernet controller is viewed in detail
- The training highlights data flows between PCI and DDR SDRAM

### RELATED COURSES

- CAN bus (002601A)
- PCI bus (002596A)
- USB bus (002606A)
- C for real-time and embedded applications (002603A)

### PARTNERS

- This training course is approved by FREESCALE

### PREREQUISITES

- Experience of a microcontroller is recommended
- Knowledge of CAN, PCI and USB busses is recommended

**WIND RIVER**

### Contact

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Course also available  
customized

Next sessions, see : <http://www.mvd-fpga.com/en/formationsCalend.html>

### TOPICS

#### MPC52xx OVERVIEW

- Innovative IO subsystem
- Dual external bus architecture : SDRAM bus and LocalPlus bus
- Bestcomm features
- Memory map, internal register space

#### 603e CORE

- 603e pipeline
- Branch management : static prediction
- Guarded memory
- 603e L1 cache : LRU algorithm, HID0 programming interface
- Software L1 data cache flush, Cache coherency basics
- JTAG debugger, hardware breakpoint vs software breakpoints
- Branch instructions
- The system call communication path between applications and RTOS
- FPU operation
- The EABI, Code and data sections, small data areas benefits
- Cache related instructions
- PowerPC timers : TB and DEC
- MMU goals : The PowerPC address processing
- WIMG attributes definition, page and block access rights definition
- Process protection through VSID selection
- TLB organization, TLB software management
- MMU implementation in real-time sensitive applications
- Exception management, Requirements to support exception nesting

#### SYSTEM INTEGRATION UNIT

- Interrupt Controller routing scheme
- General purpose IO, pin multiplexing
- General purpose Timers
- Slice timers, generation of periodic interrupts
- Real-Time Clock

#### HARDWARE IMPLEMENTATION

- Reset configuration
- Clock domains
- Power management
- DDR SDRAM basics, The DDR SDRAM controller, pinout
- Power-up initialisation, use of the I2C interface
- Initialization of memory controller registers according to a micron DDR SDRAM devices
- External bus interface, modes of operation muxed or non muxed
- Connection to ATA and PCI compliant devices as well as memory-mapped devices
- Chip select programming, Dynamic bus sizing
- DMA interface
- XLB arbiter, prioritisation, bus grant mechanism

#### USB CONTROLLER

- Data transfer types
- Host Controller interface
- OHCI specification, communication channels
- Root hub partition

#### CAN CONTROLLER

- The MSCAN controllers, clock system
- Message buffers structure
- ID bit masking, Arbitration, Timing and synchronization
- Error management, Interrupt driven operation

#### SPI CONTROLLER

- Baud rate selection, transfer delays
- Double-buffered operation
- Transmit and receive sequences

#### BESTCOMM

- SmartDMA modules, local buffer memory
- Servicing many data streams with individual latency and processing requirements
- Chaining scatter / gather capability
- Task descriptor table, Function descriptor table

#### PCI CONTROLLER

- Supported clock ratios
- PCI commands supported as a target and as a master
- XL bus initiator interface
- Endian translation
- XL bus target interface
- Multi-channel DMA transmit and receive interface
- Access to the configuration space
- Programming of inbound and outbound windows
- PCI agent vs PCI host operation mode

#### ATA CONTROLLER

- Asynchronous ATA basics, overview of ATA standards
- ATA host controller operation
- Signals and connections
- Sector addressing
- Ultra DMA protocol

#### FAST ETHERNET CONTROLLER

- MII transfers
- FIFO interface
- Address recognition
- Full and half duplex operation
- Initialization sequence
- MIB block counters

#### PROGRAMMABLE SERIAL CONTROLLERS

- PSC in UART, Codec, AC97, and Infrared SIR, MIR or FIR mode
- FIFO system

#### I2C CONTROLLER

- I2C protocol basics
- Transfer timing diagrams, SCL and SDA pins
- Clock synchronization and arbitration
- Transmit and receive sequences

### DOCUMENTATION

- Training manuals will be given to attendees during training in print.