

S12X IMPLEMENTATION IN METROWERKS ENVIRONMENT

Ref : 004034A

Duration : 3 days

OBJECTIVES

- The course has been designed by MVD so that attendees become familiar with both the MCU itself and the Metrowerks IDE
- Regarding on-site trainings only, we propose an extra consultancy day, during which input / output drivers will be generated
- The course covers the hardware implementation of the S12X, particularly the connection of external memories / IOs

RELATED COURSES

- The 2-day CAN bus training (reference 002601A) is recommended for persons involved in development of a MSCAN driver
- The training called Language C for real-time and embedded applications is recommended for persons in charge of low level programming (course 002603A)

PREREQUISITES

- Basic knowledge about processors

PARTNERS

- This training course is approved by FREESCALE



Contact

Tel : 05 62 13 52 32
Fax : 05 61 06 72 60
training@mvd-fpga.com

Course also available
customized

TOPICS

INTRODUCTION TO S12X

- S12X capabilities and target applications
- Benefits of dual core solution and consequences for the end user
- Simplifying the software development by using the Metrowerks IDE
- S12X microcontrollers architecture
- S12X derivatives
- Compatibility with S12 MCUs
- Modes of operation
- Memory mapping control
- IO pins initialization

INFRASTRUCTURE

POWER, CLOCKING AND RESET

- Voltage regulator, power on reset circuit
- PLL operation
- Reset operation
- Pierce oscillator, gain control
- COP configuration
- Low power modes

PORT INTEGRATION MODULE

- External signal description
- Memory map and register definition
- Expanded bus pin functions

INTERNAL MEMORIES

- EEPROM module
- Flash modules
- RAM module
- Protecting memory regions against writes

EXTERNAL BUS INTERFACE

- Selecting 3.3 or 5 V operation
- Stretched external bus accesses
- Data select and data direction signals
- Normal expanded modes
- Connecting external flash and SRAM to the S12X

DEBUGGING A MULTI-CORE SYSTEM

- Communicating with embedded debugger through BDM

- Enabling and activating BDM
- Instruction tracing
- Hardware breakpoints
- Tagging

PROCESSORS CORE AND MULTIPROCESSOR MECHANISMS

S12 CORE

- Programming model
- Instruction classes
- Detail of load / store, branch and system control assembly instructions
- Parameterizing compiler and linker
- Understanding sections to interface C to assembly programs

XGATE CORE

- Programming model
- Instruction classes
- Detail of load / store, branch and system control assembly instructions
- Thread execution
- Parameterizing compiler and linker
- Understanding sections to interface C to assembly programs

S12 AND XGATE INTERACTION MECHANISMS

- Interrupt steering logic
- Inter-processor interrupts
- Accessing shared resources, semaphore management
- Interrupt prioritization
- Wake up from stop or wait mode

SECURITY [On demand]

- Reprogramming the security bits
- Complete memory erase

INTEGRATED INPUTS / OUTPUTS

TIMERS

- Enhanced capture timers
- Periodic Interrupt Timer
- Pulse width modulators,

ANALOG-TO-DIGITAL CONVERTER

- External trigger pins
- Analog circuitry
- Digital sub-block

COMMUNICATION CONTROLLERS

- IICV2
- MSCANV3 controller
- Serial Communication Interface
- Serial Peripheral Interface

DEVELOPMENT METHODOLOGY

- Adapting the configuration of the S12X to satisfy the end user requirements
- Subcontracting data transfers (DMA like) to XGATE
- Using the XGATE as a arithmetical coprocessor
- Subcontracting the management of real time peripherals to XGATE
- Controlling the S12 task scheduling through XGATE

DOCUMENTATION

Training manuals will be given to attendees during training both in pdf and in print.

CONTACT INFORMATIONS

Web site : <http://www.mvd-fpga.com>

E-mail : training@mvd-fpga.com

Tel : +33 (0) 5 62 13 52 32

Fax : +33 (0) 5 61 06 72 60