

OBJECTIVES

- Give to the project manager an in depth presentation to be able to use efficiency all the resources of the component
- Give to the developer a good understanding to set up easily all the internal functions
- Study the global architecture in details : (everything concerning the user is covered)
 - ✓ To obtain the best performance based on the different flows of data crossing the XBAR, the help of numerous DMA channels and a powerful interrupt controller
 - ✓ To manage power
 - ✓ To use efficiently all the protection mechanisms and secure resources for your algorithms

PREREQUISITES

- Experience of a microcontroller is recommended
- This training is adapted to the electronics and programmers engineers confronted with the problems of the implementation of this processor

PARTNERS

- This training course is approved by Freescale


WIND RIVER

Contact

Tel : 05 62 13 52 32
 Fax : 05 61 06 72 60
 training@mvd-fpga.com

Course also available customized

RELATED COURSES

- CAN bus training (reference 002601A)
- C language for real-time and embedded applications (002603A)

Next sessions, see: <http://www.mvd-training.com/en/schedule.html>

TOPICS
MPC5674K OVERVIEW

- Main features and benefits of the Internal architecture
- MPC5674K position in the Freescale automotive portfolio
- 32-bit Power Architecture CPU history and goals for embedded applications
- Main features of all the internal resources

e200z7 CORES

- Differences between the new Book E Power Architecture and the classic PowerPC architecture
- Major subsystems description
- Pipeline and instructions timings
- Serialization
- Exception sources and vectors (emphasis on machine Check)
- SPE instruction set, signal processing capability, new data types
- Vector and scalar floating point
- APU descriptions
 - VLE // VolatileContext SaveRestore // Performance Monitor
- MMU description, initialization and miss exception routines
- L1 cache with ECC
- RAM / Cache partitioning
- Cache related instructions
- eABI:
 - Development tools file formats
 - Data types and alignment
 - Register usage conventions
 - Stack frame creation and organization
 - Functions parameter passing
- Core timers // Nexus emulation // Watchpoint logic
- Inter-cores Semaphores

PLATFORM
Clocking Reset BAM and initial pin configuration

- Clock management
- Reset configuration halfword
- Boot Assist Module : different boot modes
- MMU state after the BAM
- Configuration pins
- Initialization sequence

The Interrupt controller

- Architecture and Interrupt sources(internal and external)
- Software vs hardware vector mode
- Hardware acceleration for ISRs : use of 9-bit vectors
- Preemption, priority management

On-Chip Memories and Error Correction Status

- On-chip flash architecture
- Internal buffer and prefetch options
- Integrated ECC
- Sensorship protection
- Read while write operation
- Erase and program sequences
- On-chip SRAM : general purpose ECC SRAM

eDMA , Crossbar and Memory Protection

- Autonomous IO control
- Parallel memory bus architecture, concurrent accesses
- Programmable master priorities on a per-slave basis
- independent channels with link capability (Scatter/Gather functionalities)

System Timers

- Watchdog,
- PIT and API,
- RTC
- ADC synchronous triggering capabilities

Low power modes and Wake up functions

- Mode entry module and wake up resources

I/O DEVICES**DSPI**

- SPI protocol explanation, master / slave operation
- Command queue
- Flexible programming transfer attributes on a per-frame basis
- Transmit and receive sequences

eSCI

- UART basics
- Wake up mode, Double buffering
- Transmit and receive sequences
- Support for LIN master operation

The FlexCAN controllers

- CAN protocol basics
- Message buffer structure and mask registers
- Listen-only mode capability
- Receive and Transmit processes
- Error counters

The FlexRay controller

- Flexray protocol basics
- Controller main features
- Message buffer structure
- Rx FIFO
- Global mapping
- Module configuration
- Local node protocol relevant parameters
- Protocol constants
- Interrupt and error handling

FEC

- Ethernet basics, addressing, frame format, clock recovery
- MII hardware interface, autonegotiation
- The fast Ethernet controller
- Buffer management, buffer chaining
- Address filtering, use of hash tables
- Full duplex operation, flow control
- Receive and transmit sequences
- Error management
- Practical exercises

DOCUMENTATION

Training manuals will be given to attendees during training in print.